Remarks

In view of the above amendments and the following remarks, reconsideration of the objection and rejections and further examination are requested.

The specification has been amended so as to address the objection thereto. No new matter has been added. As a result, withdrawal of the objection to the specification is respectfully requested.

Claims 1-5 and 11-14 have been rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. Claims 1-5 and 11-14 have been amended so as to address this rejection. As a result, withdrawal of the rejection under 35 U.S.C. §112, first paragraph, is respectfully requested.

Claims 1-8 and 15-26 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Okayama (US 5,045,939) in view of Takabatake (US 6,320,909) and Stam (US 6,631,316). Claims 9 and 27-30 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Okayama in view of Takabatake and Stam and further in view of Maze (US 4,573,080). Claims 10 and 31-34 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Okayama in view of Takabatake and Stam and further in view of Eglit (US 6,054,980). Claim 11 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Okayama in view of Stam. Claim 12 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Masuda (US 6,791,623) in view of Stam. Claim 13 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Masuda in view of Stam and further in view of Okayama. Claim 14 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Masuda in view of Stam and Okayama and further in view of Worrell (US 6,633,344).

The above-mentioned rejections are respectfully traversed for the following reasons.

Claim 1 is patentable over the combination of Okayama, Takabatake and Stam, since claim 1 recites a clock conversion apparatus including, in part, a memory having a number of addresses that is less than a number of addresses required for storage of data corresponding to a predetermined period; a first counter circuit for counting a first clock, and generating write addresses of the memory so that the data corresponding to the predetermined period can be written into the memory over a plurality of times; and a second counter circuit for counting a second clock, and generating read addresses of the memory so that the data corresponding to the predetermined period, which have been written in the memory, can be read from the memory

over a plurality of times. The combination of Okayama, Takabatake and Stam fails to disclose or suggest the first counter circuit and the second counter circuit as recited in claim 1.

Okayama discloses an apparatus for converting a wide screen television signal into a normal screen television signal. The apparatus includes a motion detector 30 and a line memory 25 which is sufficient for storing all samples of the digital wide screen television signal in one horizontal line. For a writing operation of the memory 25, the memory 25 receives at its write clock terminal a first clock signal CK1 and at its write address port a write address WA generated by a write address counter 27. The write address counter 27 counts up in response to the first clock signal CK1. Samples stored in the line memory 25 are read out by applying a second clock signal CK2 to a read clock terminal of the memory 25 and by applying a read address RA to a read address port of the memory 25. The read address RA is generated by a read address counter 28 which counts up from a start address SA set at its preset terminal in response to the second clock signal CK2. The apparatus performs time axis expansion of the television signal by varying the frequencies of the first and second clock signals CK1 and CK2. (See column 3, line 4 – column 4, line 16 and Figure 2).

Okayama discloses an apparatus that utilizes the motion detector 30 for converting a maximum motion portion of the wide screen television signal into the normal screen television signal. The apparatus converts the aspect ratio in a video signal by performing the time axis expansion using the clock signals CK1 and CK2 having different frequencies in writing into and reading out from the memory 25, and varies a part of the video signal to be deleted according to a result of the motion detection by the motion detector 30, in which a counter is employed for taking out a single scanning line of a video signal having a narrow aspect ratio from a single scanning line of a video signal having a broad aspect ratio.

Okayama does disclose that the line memory 25 receives the first and second clock signals CK1 and CK2 for writing and reading data to/from the memory 25. However, as admitted in the rejection, Okayama fails to disclose or suggest that the memory 25 has a number of addresses that is less than a number of address required for storage of data corresponding to a predetermined period. Further, Okayama fails to disclose or suggest that the write address counter 27 and the read address counter 28 generate respective write and read addresses of the memory 25 so that data corresponding to a predetermined period can be written and read to/from the memory 25 over a plurality of times.

The present invention, as recited in claim 1, provides a clock conversion apparatus in which, when writing data of a single scanning line to a memory and reading the same from the memory, data of a single scanning line are stored into or read out from the memory having a capacity that is smaller than the data by limiting an address counter value which counts an address of the data of a single scanning line, thereby dividing the data of the single scanning line into several data portions to write the data to the memory having the small capacity, as well as to read out the data from the memory, many times. Therefore, the present invention can perform clock conversion without using the maximum number of effective pixels for a display, and is different from Okayama in makeup and operation. As a result, Takabatake and/or Stam must disclose or suggest the above-discussed features in order for the combination to render claim 1 obvious.

Regarding Takabatake, it discloses a picture decoding and display unit including a delay circuit 60 that delays a picture synchronization signal PSYNC, which is outputted from a control unit 14a, by a prescribed time, whereby a switching circuit 80 can selectively invalidate the delay provided by the delay circuit 60. The picture synchronization signal PSYNC is used to control a decoding unit 10 that decodes encoded picture data. (See column 10, lines 21-36; column 22, lines 29-65; and Figures 1 and 23).

Based on the above discussion, it is apparent that the picture decoding and display unit of Takabatake has an object similar to that of the present invention, and can reduce memory capacity. The picture decoding and display unit is constructed such that a time difference between a timing for starting decoding in the decoding unit 10 and a timing for starting display of the pixel data of the frame in a display unit 22 is equal to a period of one field and employs a memory having a capacity for storing one frame of pixel data. Therefore, only the capacity of one frame is needed for the capacity of a B picture.

On the other hand, in the present invention as recited in claim 1, when writing data of a single scanning line in the memory and reading the same from the memory, it is possible to store data of a single scanning line by using the memory having the capacity that is smaller than the data by limiting the address counter value which counts the address of the data of the single scanning line, thereby dividing the data of the single scanning line into several data portions to write the data to the memory having the small capacity and read out the data from the memory many times. Therefore, the present invention can perform clock conversion without using the

maximum number of effective pixels for a display, and is different from Takabatake in makeup and operation. As a result, Takabatake fails to disclose or suggest the above-discussed features of claim 1.

Regarding Stam, it discloses an image processing system that includes a memory 106 that has a lower number of storage locations than is needed to store all of the pixels of an image. As a result, only select pixels are stored in the memory 106. (See column 2, lines 18-23 and column 8, lines 44-61).

Stam discloses the image processing system employing the memory having fewer storage locations than the number of pixels. However, the system of Stam which reduces line data constituting a single pixel to thereby reduce the memory capacity is different from the present invention which reduces the number of addresses used for the memory to thereby reduce the memory capacity. As a result, Stam fails to disclose or suggest the above-discussed features of claim 1.

In light of the above discussion of Okayama, Takabatake and Stam, it is apparent that modifying the memories disclosed in Okayama or Takabatake with the disclosure in Stam of using a memory smaller than a total capacity would not meet the limitations of claim 1. Regarding this, Okayama uses a counter for reducing effective data, and Takabatake reduces an image memory by having a time difference between a frame decoding start timing and a display start timing for the image data of a frame, as described above. In neither of these situations is memory capacity reduced by dividing the video data into plural regions. Further, Stam stores data in a memory by reducing the data itself in advance. Therefore, it is apparent that the combination of Okayama, Takabatake and Stam fails to render claim 1 obvious. As a result, claim 1 is patentable over the combination of Okayama, Takabatake and Stam.

Further, (1) Maze, (2) Eglit, (3) Worrell, and (4) Masuda are relied upon as disclosing (1) a generator 28 having a detector 214 that supplies a reset pulse to a 10-bit address counter 202 to reset the counter 202 upon each transition of a signal R/W, (2) a comparator circuit 540 for comparing a last address generated by a write address counter 410 with a read address provided by a read address counter 440, and when the addresses are equal, generating a signal which resets the read address counter 440 to zero, (3) a memory management process for digital video data that is capable of detecting/buffering various video format schemes via a field type detector 78 located in a video input interface 12, and (4) an image display system including a video signal

processor 2, a frequency resolution conversion circuit 4 and a video output circuit 5, respectively. However, it is apparent that none of these references discloses or suggests the above-discussed features of claim 1.

As for claims 2-5, 11, 12 and 14, they are patentable over the references relied upon in the rejections for reasons similar to those set forth above in support of claim 1. That is, claims 2-5, 11, 12 and 14 each recite that data corresponding to a predetermined period (or one horizontal line) is written to and/or read from a memory having a capacity less than the predetermined period (or one horizontal line) over a plurality of times, which features are not disclosed or suggested by the references.

Because of the above-mentioned distinctions, it is believed clear that claims 1-34 are allowable over the references relied upon in the rejections. Furthermore, it is submitted that the distinctions are such that a person having ordinary skill in the art at the time of invention would not have been motivated to make any combination of the references of record in such a manner as to result in, or otherwise render obvious, the present invention as recited in claims 1-34. Therefore, it is submitted that claims 1-34 are clearly allowable over the prior art of record.

In view of the above amendments and remarks, it is submitted that the present application is now in condition for allowance. The Examiner is invited to contact the undersigned by telephone if it is felt that there are issues remaining which must be resolved before allowance of the application.

Respectfully submitted,

Satoru TANIGAWA et al.

By: _____
David M. Ovedovitz
Registration No. 45,336
Attorney for Applicants

DMO/jmj
Washington, D.C. 20006-1021
Telephone (202) 721-8200
Facsimile (202) 721-8250